Please type a plus sign (+) inside this box → [+]

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	TI-21004
First Named Inventor or Application Identifier	Theodore W. Houston
Title	BONDED SOI WITH BURIED INTERCONNECT TO HANDLE OR DEVICE WAFER
Express Mail Label No.	EL360239343US

On Page 1 of the specification, before line 1, insert –This application claims priority under 35 USC § 119(e)(1) of provisional application number **60/095,293** filed **08/04/98**.--

APPLICATION ELEMENTS

See MPEP Chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

1. [X] *Fee Transmittal Form (e.g., PTO/SB/17)* *(Submit an original, and a duplicate for fee processing)*
2. [X] Specification *[Total Pages* [15] *]* *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R&D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 USC d113)* *[Total Sheets* [1] *]*
4. Oath or Declaration *[Total Pages* [ ] *]*
   - a. [X] Newly Executed (original or copy)
   - b. [ ] Copy from a prior application (37 CFR §1.63(d)) *(for continuation/divisional with Box 17 completed)*

   [Note Box 5 below]

   - i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR §1.63(d)(2) and 1.33(b).
5. [ ] Incorporation By Reference *(useable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   - a. [ ] Computer Readable Copy
   - b. [ ] Paper Copy (identical to computer copy)
   - c. [ ] Statement verifying identical of above copies

ACCOMPANYING APPLICATION PARTS

8. [X] Assignment Papers (cover sheet & Documents(s))
9. [ ] 37 CFR §3.73(b) Statement *(when there is an assignee)* [X] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [X] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] *Small Entity Statement(s) [ ] Statement filed in prior application Status still proper and desired *(PTO/SB/09-12)*
15. [ ] Certified Copy of Priority Document(s) *if foreign priority is claimed)*
16. [ ] Other:

*A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.

17. If a CONTINUING APPLICATION, *check appropriate box and supply the requisite information below and in a preliminary amendment:*

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No: /

Prior application information: ***Examiner*** _____ ***Group / Art Unit:*** _____

18. CORRESPONDENCE ADDRESS

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Signature		Date	07/01/99

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

	Houston	Docket No.:	TI-21004
Serial No.:	TBD	Examiner:	TBD
Filed:	07/01/99	Art Unit:	TBD

For: **BONDED SOI WITH BURIED INTERCONNECT TO HANDLE OR DEVICE WAFER**

PRELIMINARY AMENDMENT

Assistant Commissioner
for Patents
Washington DC 20231

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(a)
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on:

Tommie Chambers 7-1-99
Tommie Chambers Date

Dear Sir:

Please amend the above referenced Application as follows:

In the Specification:

Page 1, before line 1, insert --This application claims priority under 35 USC §119(e)(1) of provisional application number 60/095,293 filed 08/04/98.--

REMARKS

Entry of the foregoing amendment prior to examinations is respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

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BONDED SOI WITH BURIED INTERCONNECT TO HANDLE OR DEVICE WAFER

FIELD OF THE INVENTION

This invention relates to a method and structure for making an interconnect between a device layer and a handle wafer which forms the substrate through a buried oxide for bonded silicon on insulator (SOI) structures.

BRIEF DESCRIPTION OF THE PRIOR ART

In the fabrication of bonded SOI devices, the normal process flow includes forming of an electrically insulating layer over a device wafer with bonding of the electrically insulating layer to a handle wafer which forms the substrate. The device wafer is then thinned down to a device level thickness.

It is known that two essentially coplanar surfaces of layers of silicon and/or silicon dioxide which are in contact with each other can be bonded together by first placing the two layers in contact with each other whereby the two layers are held together by van der Waals forces. The bond strength is increased by applying an annealing step which apparently causes some migration of atoms between the two layers in the immediate region of the contacting surfaces to cause the bonding. This procedure has been used to fabricate bonded silicon on insulator (SOI) structures with devices formed in

the device silicon layer separated by a silicon dioxide layer from the substrate silicon layer with each of the silicon layers being coplanar with opposing surfaces of the silicon dioxide layer with the bond interface at either of the silicon/silicon dioxide interfaces or within the silicon dioxide layer. Preferably, the bond interface is at the substrate/silicon dioxide interface. Structures such as interconnect may be included within the silicon dioxide layer, and dopant may be implanted into the substrate through the device and silicon dioxide layers.

In the prior art, whenever connection was to be made between the device layer and the substrate, the procedure has involved initial etching through an area of the device layer with subsequent etching through the electrically insulating layer to the substrate. Interconnect material would then be formed in the etched away region. This procedure takes up device surface area and requires the ability to reliably form the interconnect in the etched vias extending through both the device layer and the electrically insulating layer which can be difficult for thick dielectric layers. In addition, since fabrication takes place from the outer surface of the device layer, it is not possible to have a connection to just the inner surface of the device layer. Furthermore, there is no provision for utilizing the electrically insulating layer for anything other than as a dielectric separator.

SUMMARY OF THE INVENTION

In accordance with the present invention, there is provided a method and structure whereby not only is there provided an easily fabricated interconnect between the device layer and the substrate, but, in addition, there is the capability of providing buried structures within the electrically insulating layer connecting to both the substrate and the device layer without consuming outer surface area of the device layer.

Briefly, a dielectric layer is formed on the handle wafer and/or the device wafer. Interconnect structures are included in the dielectric layer(s), optionally connecting to the device wafer of handle wafer, and optionally extending to the outer surface of the dielectric layer. There is flexibility to form interconnect with high aspect ratio (depth to cross-sectional area) traversing the dielectric layer. Optionally, device and/or alignment structures may be formed in the device wafer, dielectric layer(s), or handle wafer. The bonding surfaces are planarized as necessary, such as with spin on glass (SOG), resist etch back (REB) and/or chemical/mechanical polish (CMP), such that the opposing bonding surfaces are sufficiently conformal so that the van der Wall's forces described above come into play when the wafers are aligned and brought into close proximity. The bonding step then takes place by standard techniques. A portion of the device wafer is removed to provide the desired device layer thickness, again by standard techniques. Devices are then formed in the device layer.

In the above, a portion of the interconnect structure in the dielectric layer is completed at the bonding interface. Preferably, the bonding interface is between the dielectric layer and the handle wafer, and connection is made from an interconnect structure in the dielectric layer to the handle wafer. Optionally, the bonding interface is

between the dielectric layer and the device wafer, and connection is made from an interconnect structure in the dielectric layer to the device wafer. As a further option, the bonding interface is between a dielectric layer formed on the device wafer and a dielectric layer formed on the handle wafer, and connection is made between interconnect structures in each of the dielectric layers. In each case, optionally, a thin dielectric layer may be formed between an interconnect structure and the bonding interface, either inadvertently or to facilitate bonding. Then a sufficiently high voltage is applied across this thin dielectric to cause breakdown and completion of the interconnection. The voltage can be applied at any point after the bonding, including immediately after bonding, after device wafer thinning, after initial patterning of the device layer, and after packaging of the completed integrated circuit.

It can be seen that, in accordance with the current invention, there is provided a method for fabrication of SOI structures wherein electrical connection can be made across a bonding interface without requiring etching through the outer surface of the device layer. Further, there is flexibility in forming an interconnect traversing the dielectric layer.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGURE 1 is a cross sectional view of a first embodiment of a structure fabricated in accordance with the present invention;

FIGURE 2 is a cross sectional view of a second embodiment of a structure fabricated in accordance with the present invention;

FIGURE 3 is a cross sectional view in accordance with a second embodiment of the present invention;

FIGURE 4 is a cross sectional view in accordance with a third embodiment of the present invention;

FIGURE 5 is a cross sectional view in accordance with a fourth embodiment of the present invention; and

FIGURE 6 is a cross sectional view of a subsequent portion of the process flow in fabrication of the embodiments of FIGURES 4 and 5.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring first to FIGURE 1, there is shown an SOI structure in accordance with a first embodiment of the present invention. The structure includes a handle wafer 1 which forms the substrate, and electrically insulating layer 3. Optionally, the dielectric layer 3 is formed in the handle wafer and bonded to the device wafer, or formed on the device wafer and bonded to the handle wafer. The device wafer 5 and the substrate 1 may have active and/or passive devices formed therein optionally making connection to an interconnect in the electrically insulating layer. The electrically insulating layer 3 may include therein interconnect structures 7 interconnecting the device wafer 5 to the substrate 1. The electrically insulating layer 3 can also have, with or without the above described interconnect structure, passive elements 9, such as, for example, inductors, with an interconnect 11 to the device wafer 5 and/or the substrate 1 to the passive elements.

The structure of FIGURE 1 is fabricated by providing each of a handle wafer 1 and a device wafer 5. A dielectric layer 3 is formed on one of handle wafer 1 or device wafer 5, with interconnect extending to the outer surface of dielectric 3 with or without an interconnect passing entirely therethrough 7 and/or one or more passive elements buried therein 9 and/or on a surface thereof (not shown) and/or interconnect 11 between the passive elements and one or both opposed surfaces of the electrically insulating layer. Optionally, alignment marks are formed in the dielectric layer 3 and/or in the device wafer 5 and/or the handle wafer 1. The outer surface of dielectric layer 3 is planarized, such as with combined use of a flowable dielectric and CMP. The interconnect initially extending to the outer surface of dielectric layer 3 is optionally covered with a thin dielectric after planarization. Also, a thin dielectric, such as a native oxide, may be

formed on the wafer to which dielectric layer 3 is to be bonded. The one of handle wafer 1 or device wafer 5 on which the dielectric is formed is then bonded to the other of the device wafer and handle wafer by standard means. The device layer 5 is then thinned back to the phantom line 13 with fabrication then continuing in standard manner to provide a completed device. The interconnect 7 will generally contact to source, drain or body regions of the device subsequently fabricated in device layer 5, or to interconnect formed on the outer surface of device layer 5. In the event a thin native oxide has developed over the device wafer 5 or the substrate 1 or the flowable dielectric insulates the interconnect in the electrically insulating layer from the substrate or device wafer, a sufficiently high voltage can be passed through the circuitry involving the interconnect 7 to cause breakdown of the native oxide or other dielectric and allow completion of the connection as is well known in the art. Optionally, the voltage can be applied prior to completion of fabrication of devices in device layer 5.

Referring to FIGURE 2 wherein like reference numbers refer to the same or similar structures, there is shown a structure which is the same as in FIGURE 1 and fabricated in the same manner except that the device layer includes a mesa portion 15 of the device wafer 5' which extends through the electrically insulating layer 3' and makes contact with the substrate 1. Connection can be made directly between the substrate 1 and the device wafer 5 as well as through the electrically insulating layer 3. As shown, other interconnection between the device wafer 5' and the substrate 1 can be made with an interconnect 7 as in FIGURE 1 and other interconnect 11 and/or passive elements 9 can be formed as discussed above with reference to FIGURE 1.

For the structure of FIGURE 2, silicon-to-silicon bonding can be accomplished simultaneously with the dielectric to silicon bonding. Optionally, a thin oxide may be formed in region 17 prior to bonding and subsequently broken down with application of a sufficiently high voltage.

Formation of a via through a relatively thick dielectric layer as may be used for the dielectric layer between the device wafer and the handle wafer can be difficult with standard process techniques. Forming a via or vias 7 through the dielectric 3 prior to bonding provides flexibility. One option is to form the dielectric 3 in layers with multiple levels of interconnect 11 as illustrated in FIGURE 3. Another alternative is illustrated in FIGURES 4 and 5. Dielectric layer 3 is formed, and a pattern is etched through the dielectric layer 3 to the underlying device wafer 5, forming an edge 21 where the via is to be. A sidewall of interconnect material 23 is formed on the edge as illustrated in FIGURES 4 and 5. The sidewall 23 is then selectively etched, if required, using patterned resist, leaving the interconnect material at the via location as illustrated in FIGURES 4 and 5. Additional dielectric material 25 is subsequently deposited and planarized in the via 7, as illustrated in FIGURE 6.

Various dielectric materials or composites thereof can be used to form layer 3, such as, for example, grown oxides, deposited oxides, and nitrides. Also, various conductive materials can be used to form the interconnect, such as polysilicon, amorphous silicon and tungsten. With low temperature bonding, additional materials, such as aluminum, can be used. Stacked materials, such as tungsten with titanium nitride at the interfaces can also be used. Silicides can be formed at the interconnect to wafer interface.

Though the invention has been described with reference to specific preferred embodiments thereof, many variations and modifications will immediately become apparent to those skilled in the art. For example, the invention may incorporate multiple layers of bonding. It is therefore the intention that the appended claims be interpreted as broadly as possible in view of the prior art to include all such variations and modifications.

CLAIMS

1. A method of fabricating an SOI structure which comprises the steps of:

(a) providing a substrate and a device wafer;

(b) forming an electrically insulating layer having an outer face on one of said substrate or said device wafer, said electrically insulating layer having an electrical interconnect structure therewithin, a portion of said interconnect structure extending substantially to said outer face of said electrically insulating structure; and

(c) bonding said outer surface of said electrically insulating layer to the other of said substrate or device wafer.

2. The method of claim 2 wherein a portion of said electrically insulating layer is disposed between said interconnect structure and at least one of said substrate or device wafer, further including the step of applying a voltage across said portion of said electrically insulating layer sufficient to break down said portion of said electrically insulating layer while maintaining the integrity of the remainder of said SOI structure

3. The method of claim 1 wherein at least one of said device layer and said substrate includes a bond region, said interconnect structure contacting said bond region.

4. The method of claim 2 wherein at least one of said device layer and said substrate includes a bond region, said interconnect structure contacting said bond region through said portion of said electrically insulating layer..

5. An SOI structure comprising:

(a) a device layer having a surface;

(b) a substrate;

(c) an electrically insulating layer separating said device layer from said substrate and immediately adjacent said surface of said device layer; and

(d) an electrical interconnect within said electrically insulating layer electrically connecting said substrate to said surface of said device layer.

6. The structure of claim 5 wherein a portion of said interconnect is through a broken down dielectric.

7. A method of forming an SOI structure having a device layer, a substrate and an electrically insulating layer separating a portion of said device layer from said substrate, comprising the steps of:

(a) forming a substantially planar surface comprising areas of one of said device layer and said substrate and areas of said electrically insulating layer; and

(b) bonding said surface to the other of said substrate wafer and device layer.

8. The method of claim 8 further including the step of forming an electrical interconnect structure in said electrically insulating layer, said interconnect structure contacting at least one of said device layer and said substrate.

9. The method of claim 8 further including the step of forming an electrical interconnect structure in said electrically insulating layer, said interconnect structure contacting both said device layer and said substrate.

10. A method of forming an electrically conducting via, comprising the steps of:

(a) providing a layer of electrically insulating material having a surface;

(b) forming an edge extending from said surface through said layer of electrically insulating material;

(c) forming a layer of electrically conductive material on said edge;

(d) performing a patterned etch to selectively remove electrically conductive material, leaving said material where the conducting via is desired;

(e) depositing additional electrically insulating material; and

(f) planarizing said surface.

11. The method of forming the electrically conducting via of claim 10, further including the steps of providing a device layer and a handle wafer, and separating said device layer from said handle wafer with said electrically insulating material.

12. An integrated circuit which comprises:

(a) a device layer;

(b) a substrate spaced from said device layer;

(c) a buried dielectric having an interconnect, said dielectric bonded to one of said device layer and said substrate to form an interface with said one of said device layer and said substrate; and

(d) an electrically conductive path across said interface and disposed directly beneath said device layer.

13. The circuit of claim 12 wherein said electrically conductive path contacts the other of said device layer and said substrate.

14. The circuit of claim 12 wherein said electrically conductive path is an extension of said device layer.

15. The circuit of claim 13 wherein said electrically conductive path is an extension of said device layer.

16. The circuit of claim 12 wherein said substrate is a semiconductor substrate.

17. The circuit of claim 12 wherein said substrate comprises a semiconductor substrate and a dielectric.

18. A method of fabricating an integrated circuit which comprises the steps of:

(a) providing a device layer;

(b) providing a substrate spaced from said device layer;

(c) bonding a buried dielectric having an interconnect therein to one of said device layer and said substrate to form an interface with said one of said device layer and said substrate; and

(d) forming an electrically conductive path across said interface to said interconnect directly beneath said device layer.

19. The method of claim 18 wherein said electrically conductive path contacts the other of said device layer and said substrate.

20. The method of claim 18 wherein said electrically conductive path is an extension of said device layer.

21. The method of claim 19 wherein said electrically conductive path is an extension of said device layer.

22. The method of claim 18 wherein said step of forming an electrically conductive path across said interface to said interconnect is formed by breakdown of said dielectric.

23. The method of claim 18 wherein said substrate is a semiconductor substrate.

24. The method of claim 18 wherein said substrate comprises a semiconductor substrate and a dielectric.

ABSTRACT OF THE DISCLOSURE

A method of fabricating an electrically conductive via and an SOI structure and the structure. A substrate and a device wafer are provided and an electrically insulating layer having an outer face is formed on one of the substrate or device wafer. The insulating layer has an electrical interconnect structure therein, a portion extending to the outer face of the insulating structure. The outer surface of the insulating layer is bonded to the other of the substrate or device wafer. A portion of the insulating layer can be disposed between the interconnect structure and at least one of the substrate or device wafer with ultimate interconnection made by applying a voltage across the portion of the insulating layer sufficient to break down the portion of the insulating layer while maintaining the integrity of the remainder of the SOI structure. At least one of the device layer and substrate includes a bond region with the interconnect structure contacting the bond region. A portion of the interconnect structure can be buried within the insulating layer as a separate layer therein. As an alternate embodiment, a planar surface can be formed having areas of the device layer and areas of the insulating layer and that surface can be bonded to a substrate wafer. As a still further embodiment, a layer of electrically insulating material is formed having a surface and an edge is formed extending from the surface through the layer of insulating material. A layer of electrically conductive material is formed on the edge and a patterned etch is provided to selectively remove the conductive material from the edge, leaving the material where the conducting via is desired. Then additional insulating material is deposited and the surface is planarized.

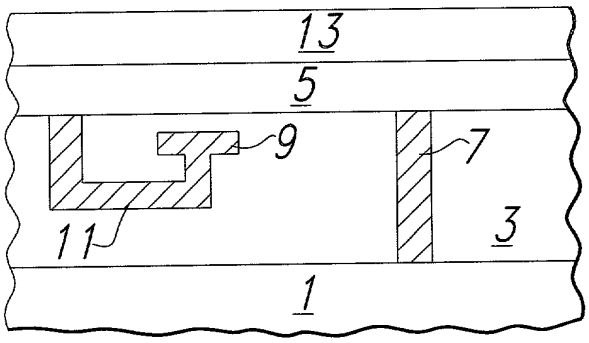

Fig.1

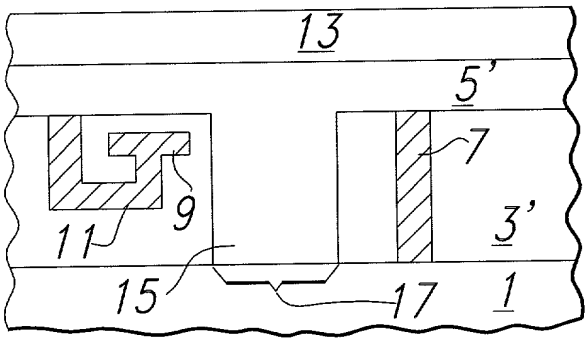

Fig.2

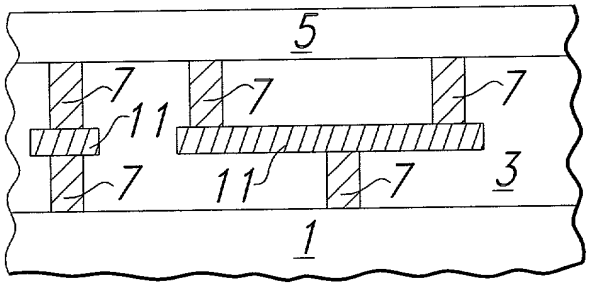

Fig.3

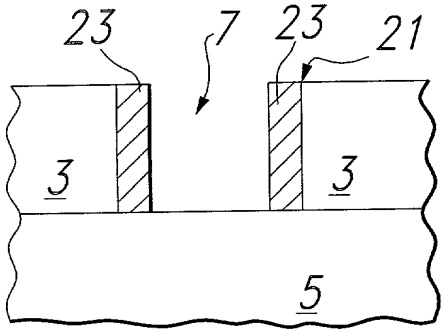

Fig.4

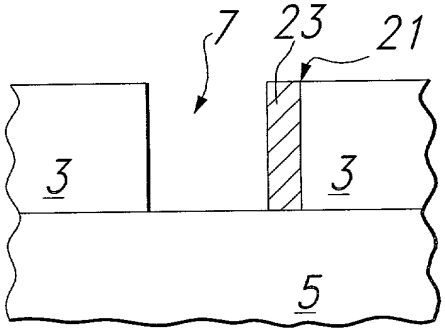

Fig.5

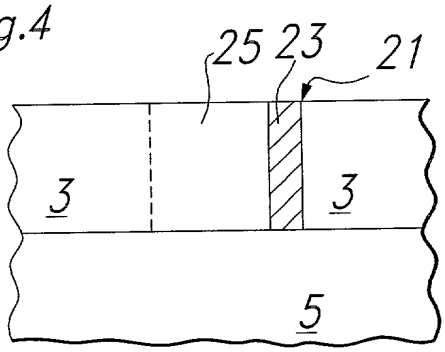

Fig.6

ATTORNEY'S DOCKET NO.
TI-21004

APPLICATION FOR UNITED STATES PATENT

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor if only one name is listed below, or an original, first and joint inventor if plural inventors are named below, of the subject matter which is claimed and for which a patent is sought on the invention entitled as set forth below, which is described in the attached specification; that I have reviewed and understand the contents of the specification, including the claims, as amended by any amendment specifically referred to in the oath or declaration; that no application for patent or inventor's certificate on this invention has been filed by me or my legal representatives or assigns in any country foreign to the United States of America; and that I acknowledge my duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, section 1.56;

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

TITLE OF INVENTION: **BONDED SOI WITH BURIED INTERCONNECT TO HANDLE OR DEVICE WAFER**

POWER OF ATTORNEY: I HEREBY APPOINT THE FOLLOWING ATTORNEYS TO PROSECUTE THIS APPLICATION AND TRANSACT ALL BUSINESS IN THE PATENT AND TRADEMARK OFFICE CONNECTED THEREWITH

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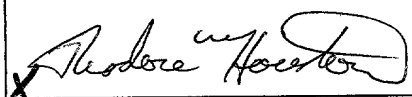
Post Office Address **1522 North Cheyenne Dr.** **Richardson, TX 75080**	Post Office Address	Post Office Address
COUNTRY OF CITIZENSHIP: **USA**	COUNTRY OF CITIZENSHIP:	COUNTRY OF CITIZENSHIP:
SIGNATURE OF INVENTOR: X 	SIGNATURE OF INVENTOR:	SIGNATURE OF INVENTOR:
DATE: 7/21/98 X	DATE:	DATE: